Technical Note

SOAP - Project (FPGA Interface with MOSFET in B2B Topology)

ANalog Application memriSTOR Program

JP Guarrera - Tuesday, 19 January 2021
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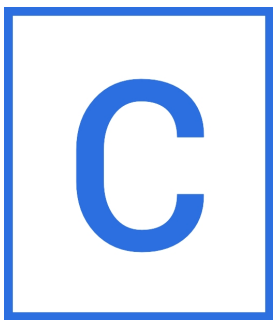

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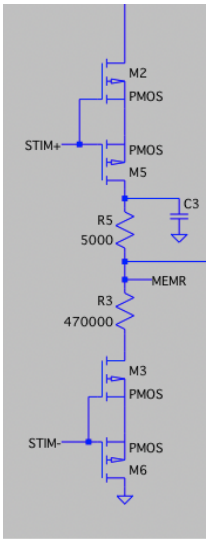
1. Background

Since 2020 , Conceptualise is investigating memristors world. Starting with Digilent AD2 oscilloscope device, we figured out a lot of limitation of this device to explore in timing details memristors behaviour. To overcome this limitation the FPGA is used as the main timing coordinator . In addition, memristors needs driving circuitry as analog switch or muxes for programming , erasing and be used in the application circuit. The main issue for classic analog switch or muxes are speed limitation, capacitive effect & size. We based our development on MOSFET Back to Back topology which is offering a design stage with only 2 transistors & 2 discrete components.

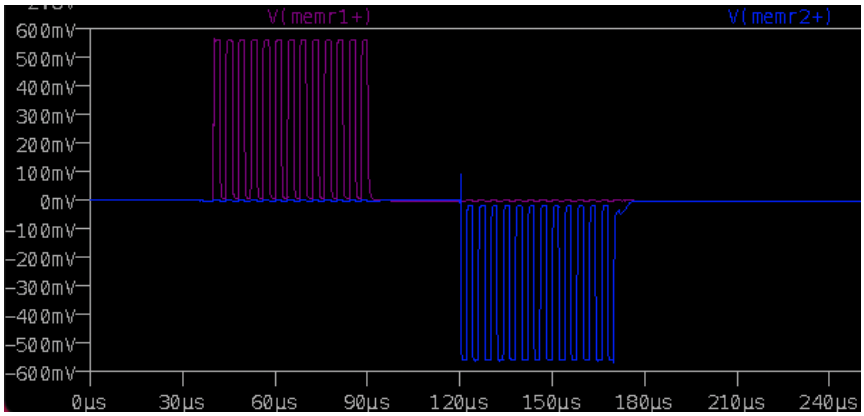
2. The MOSFET Back to Back Topology

The mosfet back to back topology is described in the figure below



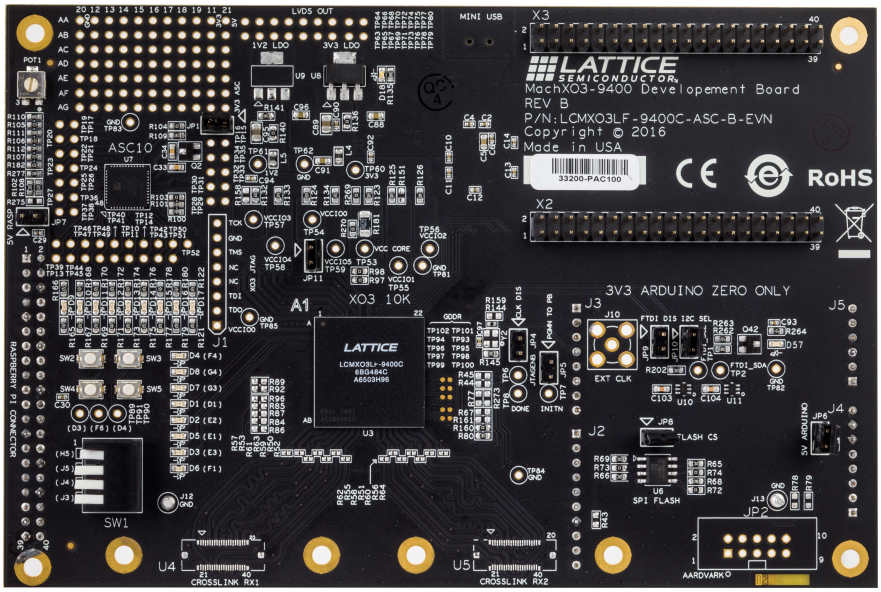
The topology can be used as illustrated from top & bottom of the memristor (Crossbar application) or only on top (simple application like SOAP project). The current limitation resistor and a decoupling capacitor are included. The main problem with the B2B stage is the precise MOSFET point of commutation that will be fully covered by the FPGA. For the illustration of the simulation, we used a resistor of 470K instead of complex memristor model. 470K is the worst case value for timing performance.

The next figure shows a simulation plot under LTSPICE & highlights the timing performance of the stage (pulses of 2us , but can be lowered to 500ns). Positive pulses on Memristor 1 (programming) Negative pulses of Memristors 2 (Erasing)



3. Native Lattice MACHX03 Board

Before creating our own board including full driving stage & fpga, we preferred to validate the concept with the usage of FPGA evaluation board from LATTICE.
The board offered a powerful FGPA, lots of direct I/O (X2 & X3 connectors) and a programming interface by USB (bottom side).



https://www.latticesemi.com/products/developmentboardsandkits/machxo39400devboard

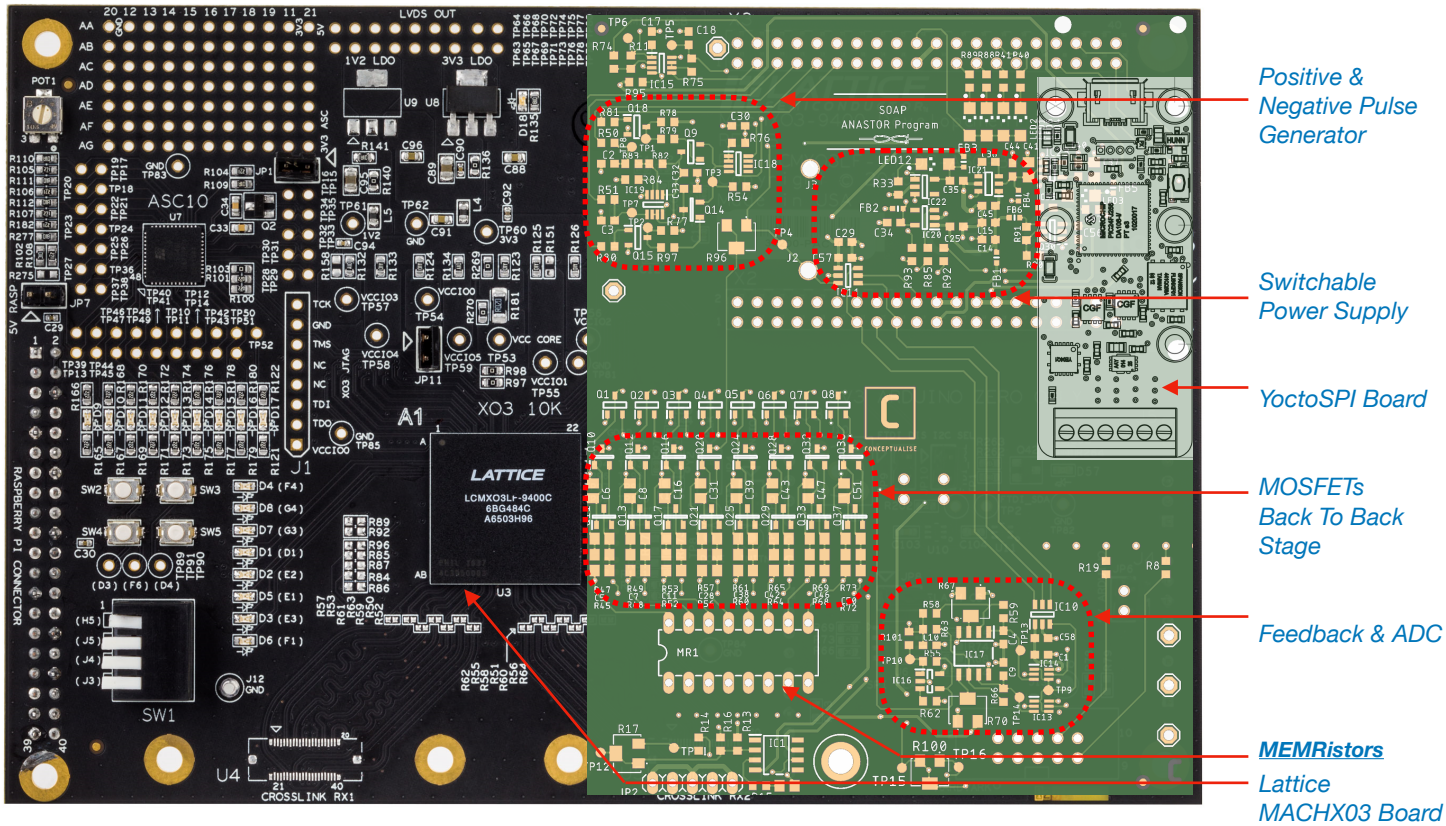
The LATTICE programming suite is free and can be downloaded at
https://www.latticesemi.com/Products/DesignSoftwareAndIP/FPGAandLDS/LatticeDiamond

4. Interface Board with Memristors

We designed a board to be plugged on X2& X3 connectors.
On bottom left, the placement of the DIL16 Memristors from Knomw inc.
https://knowm.com/collections/frontpage/products/m-sdc-memristor-8-discrete-16-dip

We include switchable power supplies , to allow the fpga to take the full control of the power applied to all driving stage .
On the TOP Left, the positive & negative pulse generator is designed to provide pulses of min 500ns at +/-2.5V on the memristors.
We added the YoctoSPI Board to provide to end user the access to raw data with a simple python script.
https://www.yoctopuce.com/EN/products/interfaces-electriques-usb/yocto-spi

The full power of the setup is provided by the USB (bottom side)



5. FPGA Description & Application SW

The FPGA architecture & description will be soon released & the Application SW will be based on python script.